

Microwaves & RF

FOR DESIGNS AT HIGHER FREQUENCIES

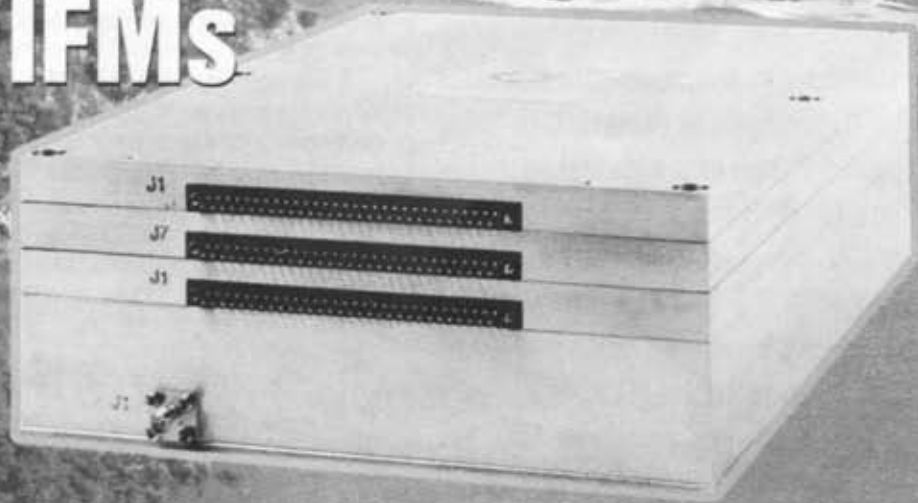
A PENTON PUBLICATION • JUNE



FAST CLOCK RATES ACCELERATE IFMS

Plus...

- Dual-use markets
- ADCs and phase noise
- Amplifier IMD predictions



Special Section:
Software Solutions

Cover Feature

HIGH CLOCK RATES ADVANCE IFM/DFD TECHNOLOGY

An IFM receiver with a 40-MHz clock rate captures pulsed signals as fast as 50 ns over a 70-dB dynamic range.

FAST frequency measurements are vital to electronic-warfare (EW) systems. Many such systems rely on instantaneous-frequency-measurement (IFM) receivers to capture high-speed pulsed signals over wide instantaneous bandwidths (particularly in dense pulse-signal environments) as well as to provide digitized data for analysis of frequency, amplitude, pulse width, and pulse time of arrival (TOA). While such receivers have been available for many years, recent advances from Wide Bank Systems (Rockaway, NJ) promise improved performance and faster operating speeds.

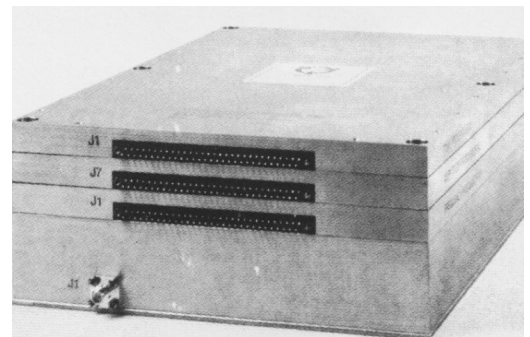
IFM receiver technology is based on the use of a parallel array of microwave correlators to capture and process incoming RF data. This array and portion of the receiver is usually identified as the digital frequency discriminator (DFD). In addition to this array, a parallel channel provides digital RF

WILLIAM B. SULLIVAN, President, Wide Band Systems, Inc., P.O. Box 389 Franklin Ave, Rock-away, NJ 07866-0289; (973) 586-6500, FAX: (973) 627-9190

amplitude data, which is used in the measurement of pulse width and TOA.

First-generation IFM receivers were triggered devices, detecting the presence of RF signals then beginning a conversion process to digitize those signals to derive the parametric data. This approach suffered from large shadow times (during which signals went undetected, allowing threats to go unnoticed). This long shadow time was needed to allow the processing circuits to recover following a measurement. These early systems also suffered difficulty in identifying the beginning and end of an RF pulse based on either 3- or 6-dB points of the RF envelope. This latter problem, because the conversion process had to begin at a particular RF input power level, was particularly apparent when the IFM receiver was processing RF pulse envelopes with slow rise and fall times.

An IFM receiver with a 20-MHz clock rate was developed in the late 1970s. This second-generation design offered reduced shadow time, accommodated slow RF-envelope rise and fall times, and provided the capability to digitally process intrapulse parameters, such as frequency modulation on

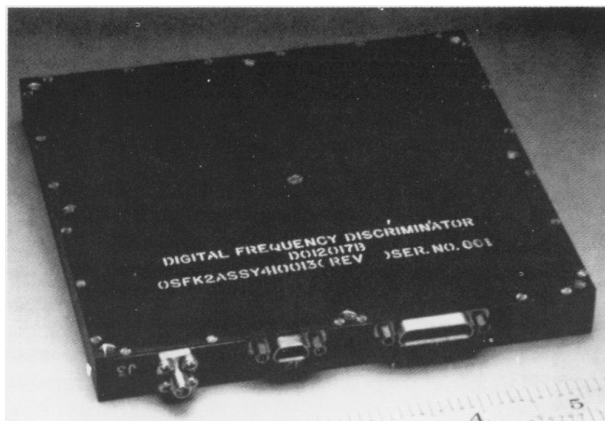


1. Using a 40-MHz internal clock rate, the latest generation of IFM receivers can achieve pulse TOA resolution of 25 ns.

pulse (FMOP) and phase modulation on pulse (PMOP). While this design represented a successful development, the 20-MHz clock rate (due to device limitations) restricted signal capture to one sample every 50 ns. This limited the receiver to processing minimum RF pulse widths of 100 ns for 100-percent probability of intercept (POI) while limiting the pulse width and TOA resolution to 50 ns.

Recent advances in digital device technology, particularly the availability of 50-MHz clocked TTL flash analog-to-digital converters (ADCs) and 8-kb X 8-b TTL programmable read-only-memory (PROM) chips with

IFM RECEIVER



2. The heart of the new IFM receiver is a clocked digital frequency discriminator (DFD).

access times of 20 ns, have led to the third generation of IFM receivers (Fig. 1). The improved clock rate allows the receiver to operate at a clock rate of 40 MHz, capturing one signal sample every 25 ns.

While the 40-MHz IFM receiver clock rate provided the obvious extension of the minimum RF pulse width for 100-percent POI to 50 ns and immediately improved the pulse width and TOA resolution to 25 ns, the increased clock rate, in combination with other parallel digital developments, gave access to new dimensions in real-time RF-signal-parameter encoding. This new processing power provides 1-ns TOA resolution, sample-by-sample estimation of RF signal-to-noise ratio (SNR) and data-encoding quality, and the ability to provide frequency association of a series of non-contiguous RF pulsed inputs.

At the heart of the 40-MHz processing is the clocked DFD, which provides a parallel digital frequency measurement every 25 ns (Fig. 2). This frequency data is error-corrected, suppressing correlator phase errors. The DFD is also temperature-corrected to remove the effects of temperature on the coaxial delay lines associated with each correlator. The DFD includes error detection to flag errors due to, for example, the presence of multiple simultaneous signals.

The 40-MHz clocked DFD employs a coherent threshold circuit to provide a sample-by-sample estimate of RF SNR. This capability allows the IFM receiver to quickly (in only 25 ns) adapt to changes in the RF noise level in signals entering the receiver. In applications where the IFM receiver serves as a baseband processor for a

host receiver system that switches the RF front-end gain, noise figure, or bandwidth, the IFM immediately adapts to this new noise level, allowing the host system to switch from band to band without settling delays from the IFM receiver.

Digital noise-riding threshold circuits were employed in earlier IFM receivers to detect noise levels. Unfortunately, these circuits required 6-ms integration time after each change in noise level. The 40-MHz clocked IFM receiver can also automatically adapt to the presence of external noise, such as interference from broadband noise jammers.

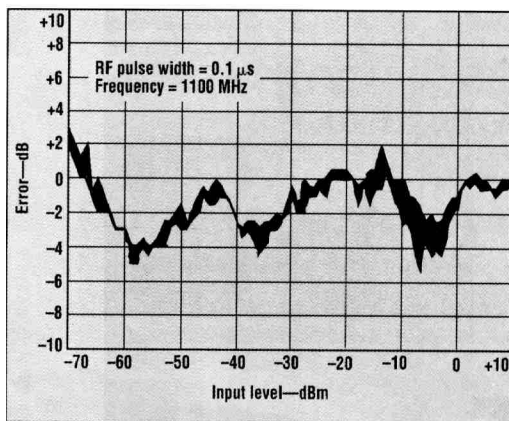
In the new IFM receiver, implementation of a 40-MHz clocked digital amplitude quantizer (DAQ), accurate over wide bandwidths and exhibiting instantaneous dynamic range in excess of 70 dB, posed special problems. Merely digitizing the video output of an extended-range successive-detection log video ampli-

fier (SDLVA), while the most obvious approach, presented problems with the video waveform. These problems related first to the fidelity of the video representation in terms of video overshoot and frequency recovery time and, second, to the time relationship between the digitized amplitude video and the digitized frequency data.

Video overshoot introduced an amplitude-dependent error in the measurement of peak RF-envelope amplitude and, in extreme cases, also introduced errors in the measurement of the 3- or 6-dB RF-envelope pulse width. An ideal RF amplitude quantizing circuit follows the RF envelope accurately, particularly during the rise and fall time. Without RF bandwidth restrictions, the amplitude quantizer will ideally provide a rectangular video output. When the RF and/or video bandwidth is restricted, the video envelope exhibits exponential rise/fall characteristics.

This exponential fall time asymptotically approaches the quiescent video level, as determined by the RF input SNR. The slow rate of the exponential video fall time may either mask the existence of a second low-level RF input signal or may cause the receiver to falsely indicate that such a signal exists. When subsequent signals are masked in time due to the use of a narrow RF bandwidth, there is very little that the video processor can do to improve the situation. It is a design flaw when the video circuits themselves cause the problem.

A second problem with the timing of the video, when using an SDLVA, is due to the time shift within the SDLVA. The SDLVA employs a cascade of RF amplifiers, each with a video detector. The video outputs of the detectors are summed to generate composite video which provides a piecewise logarithmic representation of the RF envelope. The propagation delay of each of the cascaded RF amplifiers is finite and measurable. The video output of a small signal is provided by the video detector which



3. Amplitude measurement errors are generally better than ± 2 dB across an 80-dB dynamic range for a 100-ns pulse.

IFM RECEIVER

follows the entire chain of RF amplifiers. The video output resulting from a strong signal is obtained at the input to the SDLVA.

Because signals at different levels are being measured at different points along the SDLVA, there is a substantial time shift in the location of the 3-dB points of the RF input envelope over the amplifier's full dynamic range. This time shift causes obvious problems in multiple-receiver, emitter-location systems which employ TOA data. It also causes a problem in the association of RF-envelope amplitude data with RF frequency data within the clocked receiver.

Consider that the IFM receiver is pipelining RF amplitude and frequency data at a 40-MHz clock rate. If the RF input is a 50-ns RF pulse, the frequency processor may provide only one valid frequency measurement. If an SDLVA introduces any substantial error to the RF amplitude timing, the receiver may have great difficulty correctly capturing this single valid frequency measurement.

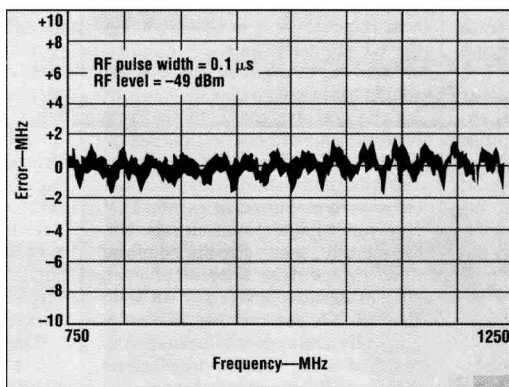
To avoid the fidelity and timing problems of the SDLVA/digitizer approach, the monolithic DAQ was developed. This circuit provides clocked digital RF-envelope data which is accurate and monotonic over wide dynamic ranges and octave or greater bandwidths. The monolithic DAQ directly converts the RF envelope into a digital logarithmic representation. If an analog log video output is desired, a digital-to-analog converter (DAC) can be employed.

The clock monotonic DAQ samples the RF envelope every 25 ns. The sampling process time-corrects the sampled date to remove the time relationship between RF amplitude and data delay. This provides a constant time location for the RF envelope's 6-dB reference points. The video bandwidth is restricted to 10 MHz, providing a video rise time of 35 ns. Very-fast RF-envelope rise times are, therefore, slowed to 35 ns. This permits multiple RF-envelope samples to be taken during the RF-envelope video rise time.

Real-time analysis of the sequence of RF-envelope amplitude samples,

taken in the region of the 6-dB points, are employed to provide accurate absolute TOA data in the subnanosecond region. This provides real-time TOA data, with nanosecond accuracy, while retaining a TTL pipeline processor clocked at 40 MHz.

The 40-MHz clocked IFM receiver is a clocked pipeline processor, allowing internal intrapulse processing to extract, for example, intrapulse frequency or phase modulation. The IFM receiver



4. Frequency measurement accuracy is rated at better than 0.5 percent of customer-specified RF bandwidths. This 750-to-1250-MHz bandwidth was checked with a 100-ns pulse.



also analyzes each data sample to estimate the instantaneous RF SNR and to estimate the probability that the sample has been distorted by the presence of an interfering simultaneous signal.

A multipath blanker is provided to suppress receiver output data in the event of local multipath. The multipath blanker examines each subsequent digital measurement for similarity to a preceding measurement within a time interval irrespective of the intervening occurrence of other unrelated signals. The degree of similarity and the processing time interval are both digitally preset with the receiver. This capability to provide real-time RF frequency-measurement association by similarity, coupled with accurate TOA processing provided on a pulse-by-pulse basis, provides the IFM receiver with the capability to resort the frequency-associated pulse-repetition interval (PRI), reducing the real-time processing

requirements of the host system computer.

The 40-MHz clocked IFM receiver offers an instantaneous dynamic range in excess of 70 dB (Fig. 3), with absolute accuracies better than 0.5 percent of the RF bandwidth for frequency measurements at customer-specified frequency ranges (Fig. 4). These receivers also provide absolute amplitude measurement accuracies of 1-dB RMS: the TOA accuracy is on the order of 1 ns. The receiver circuits are all DC-coupled without DC restoration requirements, providing 100-percent POI for RF pulse widths as narrow as 50 ns. The receiver can also process CW signals. It is designed to maintain temperature stability without heating ovens. Circuitry in the receiver measures the temperature of the delay lines associated with the microwave correlators, then applies digital correction for the output frequency data.

This array of processing capability is packaged in a single 3 X 7 X 10-in. (76 X 178 X 254-mm) module weighing less than 10 lbs. (4.5 kg) and dissipating 35 W. The use of all CMOS/TTL processing elements and attention to conductive cooling assures a high degree of reliability. **Wide Band Systems, Inc., P.O. Box 289, 389 Franklin Avenue, Rockaway, NJ 07866-0289; (973) 586-6500, FAX: (973) 627-9190.**